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**NEW QUESTION: 1** Which of the following describes a computer processing architecture in which a language compiler or pre-processor breaks program instructions down into basic operations that can be performed by the processor at the same time? **A.** Super Scalar Processor Architecture (SCPA) **B.** Very-Long Instruction-Word Processor (VLIW) **C.**

Reduced-Instruction-Set-Computer (RISC) **D.** Complex-Instruction-Set-Computer (CISC)

**Answer: B** Explanation: Very long instruction word (VLIW) describes a computer processing architecture in which a language compiler or pre-processor breaks program instruction down into basic operations that can be performed by the processor in parallel (that is, at the same time). These operations are put into a very long instruction word which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit. The following answer are incorrect: The term "CISC" (complex instruction set computer or computing) refers to computers designed with a full set of computer instructions that were intended to provide needed capabilities in the most efficient way. Later, it was discovered that, by reducing the full set to only the most frequently used instructions, the computer would get more work done in a shorter amount of time for most applications. Intel's Pentium microprocessors are CISC microprocessors. The PowerPC microprocessor, used in IBM's RISC System/6000 workstation and Macintosh computers, is a RISC microprocessor. RISC takes each of the longer, more complex instructions from a CISC design and reduces it to multiple instructions that are shorter and faster to process. RISC technology has been a staple of mobile devices for decades, but it is now finally poised to take on a serious role in data center servers and server virtualization. The latest RISC processors support virtualization and will change the way computing resources scale to meet workload demands. A superscalar CPU architecture implements a form of parallelism called instruction level parallelism within a single processor. It therefore allows faster CPU throughput than would otherwise be possible at a given clock rate. A superscalar processor executes more than one instruction during a clock cycle by simultaneously dispatching multiple instructions to redundant functional units on the processor. Each functional unit is not a separate CPU core but an execution resource within a single CPU such as an arithmetic logic unit, a bit shifter, or a multiplier. Reference(s) Used for this question: [http://whatis.techtarget.com/definition/0,,sid9\\_gci214395,00.html](http://whatis.techtarget.com/definition/0,,sid9_gci214395,00.html) and <http://searchcio-midmarket.techtarget.com/definition/CISC> and <http://en.wikipedia.org/wiki/Superscalar>

**NEW QUESTION: 2** You deploy an Azure Application Gateway. You need to ensure that all the traffic requesting <https://adatum.com/internal> resources is directed to an internal server pool and all the traffic requesting <https://adatum.com/external> resources is directed to an external server pool. What should you configure on the Application Gateway? **A.** multi-site listeners **B.** SSL termination **C.** basic routing **D.** URL path-based routing

**Answer: D** Explanation: URL Path Based Routing allows you to route traffic to back-end server pools based on URL Paths of the request. In the question there are two different path from where the traffic is getting generated as below <https://adatum.com/internal> <https://adatum.com/external> So in this case we can use URL path-based routing feature of Application Gateway. Reference: <https://docs.microsoft.com/en-us/azure/application-gateway/url-route-overview>

**NEW QUESTION: 3** **A.** Option C **B.** Option B **C.** Option D **D.** Option A **Answer: D**

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